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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,033	06/24/2003	Tetsuya Shigeta	041465-5192	9552

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MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
WU, XIAO MIN	
ART UNIT	PAPER NUMBER
2674	

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,033	SHIGETA ET AL.	
	Examiner	Art Unit	
	XIAO M. WU	2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-13,22-27 and 33-56* is/are allowed.

6)☒ Claim(s) *1-3,5,6,14,17,18,20,28,29 and 31* is/are rejected.

7)☒ Claim(s) *4,7,15,16,19,21,30 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/17/04; 6/24/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 20 and 31 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 18 and 29, respectively. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-6, 14, 17-18, 20, 28-29 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Nagai et al. (US 2002/0005863)

As to claim 1, Nagai discloses A display panel drive device (Fig. 3) comprising: a parallel-to-serial converter (161) for conducting parallel-to-serial conversion on an input signal (e.g. image data, Fig. 3) and outputting a serial signal; a transmission section (152, Fig. 3) for converting the serial signal output from the parallel-to-serial converter (161) to a signal complying with a differential serial transmission system and transferring a signal via a transmission line; a reception section (153, Fig. 3) for receiving the signal transferred via the

transmission line; a serial-to-parallel converter (181) for conducting serial-to-parallel conversion on the signal received by the reception section (153) and outputting a parallel signal; and a drive pulse output section (e.g. RGB data 24 bit, see Fig. 6) for generating a drive pulse to drive a display panel based on the parallel signal output by the serial-to-parallel converter.

As to claim 2, Nagai discloses the input signal (image data) comprises drive pulse generation control data (e.g. 24-bit RGB image data) and a clock (151).

As to claim 3, Nagai discloses a display control section (151, 152, Fig. 3) for controlling display on a display panel (155, Fig. 3); a drive section (153, Fig. 3) for driving the display panel based on a signal supplied from the display control section; and a data transfer device (152, Fig. 3) for transferring data between the display control section (151, 152) and the drive section (153), wherein the data transfer device comprises the parallel-to-serial converter (161) and the transmission section (154), and the drive section (153) comprises the reception section (153) and the serial-to-parallel converter (181).

As to claim 5, Nagai discloses the input signal comprises the address data (e.g. different channels for red, green and blue data) and drive pulse generation control data (e.g. clock signal generated by the graphics controller).

As to claim 6, Nagai discloses a display control section (151) for controlling display on a display panel; a drive section (153) for driving the display panel based on a signal supplied from the display control section; and a data transfer device (152) for transferring data between the display control section (151) and the drive section (153), wherein the data transfer device comprises the parallel-to-serial converter (161) and the transmission section (154), and the drive section (153) comprises the reception section (153) and the serial-to-parallel converter (181).

As to claim 14, Nagai discloses a display panel drive device comprising a memory (151, Fig. 3) for storing display control data, a readout device for reading out the display control data (e.g. Control signal, Fig. 3) from the memory based on a first clock (e.g. Clock signal, Fig. 3) having a first frequency, a data transfer device (152) for transferring the display control data read out by the readout device, and a display panel drive section (153) for driving a display panel based on the display control data transferred by the data transfer device (152), wherein a clock conversion circuit (162) is provided between the memory (151) and the data transfer device (152).

As to claim 17, Nagai discloses a display control device having a display control section (151, 152) of a display panel drive device comprising a display control section (151, 152) for controlling display on a display panel, a drive section (153) for driving the display panel (155) based on a signal supplied from the display control section, and a data transfer device (152) for transferring data between the display control section (151) and the drive section (153), wherein the data transfer device (152) comprises in the display control section (151, 152): a parallel-to-serial converter (161) for conducting parallel-to-serial conversion on an input signal and outputting a serial signal; and a transmission section (154) for converting the serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring a signal toward the drive section via a transmission line (154), and the data transfer device comprises in the drive section: a reception section (153) for receiving the signal transferred via the transmission line (154); and a serial-to-parallel converter f(182) or conducting serial-to-parallel conversion on the signal received by the reception section.

As to claims 18, 20, 29, 31, Nagai discloses the input signal comprises drive pulse generation control data (e.g. 24 bit digital pulse) and a clock (e.g. clock signal).

As to claim 28, Nagai discloses a drive device having a drive section of a display panel drive device comprising a display control section (151, 152) for controlling display on a display panel, a drive section (153) for driving the display panel based on a signal supplied from the display control section, and a data transfer device (152) for transferring data between the display control section and the drive section, wherein the data transfer device comprises in the display control section: a parallel-to-serial converter (161) for conducting parallel-to-serial conversion on an input signal and outputting a serial signal; and a transmission section (152) for converting the serial signal output from the parallel-to-serial converter to a signal complying with a differential serial transmission system and transferring a signal toward the drive section via a transmission line (154) , and the drive section comprises: a reception section (153) for receiving the signal transferred via the transmission line; and a serial-to-parallel converter (181) for conducting serial-to-parallel conversion on the signal received by the reception section.

Allowable Subject Matter

4. Claims 4, 7, 15-16, 19, 21, 30 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 8-13, 22-27 and 33-56 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: None of the prior arts of record alone or in combination teaches or fairly suggests the limitations of "a first PLL circuit for generating a first clock equivalent in frequency to n times an input

clock and a second clock equivalent in frequency to the input clock in synchronism with the input clock" and "a second PLL circuit for generating a third clock equivalent in frequency to n times the first clock output and transmitted from the first PLL circuit and a fourth clock equivalent in frequency to the first clock in synchronism with the first clock, and a serial-to-parallel converter for conducting serial-to-parallel conversion on the received drive pulse generation control data based on the third clock output from the second PLL circuit" as required in independent claims 8, 22, 33, 45 and 51.

7. None of the prior arts of record alone or in combination teaches or fairly suggests the limitations of "the display control section comprises a storage section for storing address data, a readout section for reading out address data stored in the storage section, and a shift clock generation section for generating a shift clock, the drive section comprises a shift register for successively storing the address data based on the shift clock, a latch circuit for latching the address data stored in the shift register, and a drive circuit for driving the display panel based on the address data output from the latch circuit, the input signal comprises the address data and the shift clock" as required in dependent claims 4, 7, 19, 21, 30 and 32

8. None of the prior arts of record alone or in combination teaches or fairly suggests the limitations of "the clock conversion circuit comprises a FIFO memory, and the display control data is written into the FIFO memory based on the first clock, and the display control data written into the FIFO memory is read out based on a second clock having a second frequency preset independently of the first clock" as required in dependent claim 15.

Conclusion

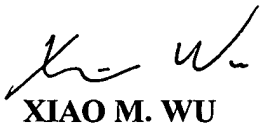
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. 6,147,672, 2002/0140662 and 2003/0016189 are cited to teach a driving circuit for a flat panel display device.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to XIAO M. WU whose telephone number is 571-272-7761. The examiner can normally be reached on 6:30 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, PATRICK EDOUARD, can be reached on 571-272-7603. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

x.w.
December 11, 2005



XIAO M. WU
Primary Examiner
Art Unit 2674